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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,771	06/23/2003	Norio Ishitsuka	500.42877X00	5732

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,771	ISHITSUKA ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *12-18 and 28-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 19-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restriction

Applicant's election with traverse of claims 1-11 and 19-27 acknowledged. The traversal is on the ground(s) that the method and device structure claims are similar. This is not found persuasive because method and product are statutorily distinct categories of invention, and the particular method claimed is distinct from the particular product claimed because there is an alternative method of making the device. Therefore, there is no reason why a search for product must include a search for the method as well. The existence of an alternative method of making the device, as well as the different classification of two inventions, provide evidence of burden on the examiner in examining both inventions. (see MPEP §§ 803.02, 806.04(a)-(j), 808.01(a) and 808.02).

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8, 10-11, 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Huang 6,406,987.

Huang discloses a semiconductor device, which includes :

semiconductor substrate 1, fig. 6-7 and col. 4, lines 49+,

an element isolating region 12 having a trench (STI) formed in said semiconductor substrate 1 and an embedding insulating film 12 which is embedded into the trench (STI),

an active region formed adjacent to the element isolating region 12, in which gate insulating 14 film is formed,

a gate electrode 16 is formed on the gate insulating film 14, col. 5, lines 4+,

a region formed in such a manner that at least a portion of the gate electrode 16 positioned on the element isolating region 12 (fig. 7), and first edge surface of an upper side of embedding insulating film 12 in a first element isolating region (left hand side of fig. 7) where gate electrode positioned is located above a second edge surface the embedding insulating film in a second element isolating region where said gate electrode film 16 (left hand side of fig. 7) is not positioned,

second edge surface is 500-1000 angstroms which is greater than the gate oxide of 40 angstroms, col. 5, lines 52+,

active region has impurity doped region 17/18,

a boundary plane (A),

an interlayer insulating film 21, fig. 8.

Claim 19 is rejected under 35 U.S.C. § 102(b) as being anticipated by Tasaka 5,561,078.

Tasak discloses a semiconductor device, which includes :

a step for forming an oxide film 2 on a semiconductor substrate1, fig. 1A+ and col. 1, lines 16+,

forming an oxidation preventing film 3 on said oxide film, 2,

a step a step removing both oxidations preventing film 3 and said oxidė film 2 of a predetermined region 6 so as to expose said semiconductor substrate 1,

a step for etching said exposed substrate 6 so as to form a trench 7,

depositing an insulating film 9 on both trench 7 and said oxidation preventing film 3,

a step of removing insulating film 9 deposited on the oxidation preventing film 3,

a step for forming a plurality of element isolating trenches into which deposited element is formed,

a gate electrode 3/11 formed via a gate insulating film 2 on a surface of an active region of semiconductor substrate,

a trench formed in element isolating region of the semiconductor substrate, which is embedded by an embedding insulating film, 9 wherein:

an upper edge of the embedding insulating film is caused retreat from the surface said active region to the side of a trench bottom portion, fig. 10-11 and col. 1, lines 44+.

Claim 22 is rejected under 35 U.S.C. § 102(e) as being anticipated by Pividori 2003/0100166.

Pividori teaches a semiconductor device comprising: a memory array constituted by a plurality of memory cells arranged on a semiconductor substrate in a matrix shape; a peripheral circuit region where a circuit element different from said plurality of memory cells is formed, and a plurality of element isolating portions made of an insulating film embedded into a trench on a major surface of a semiconductor substrate, wherein:

memory array (on left hand side of figure 2F and para. 27 and 35), a recess amount of element isolating portion is relatively large, whereas

in said peripheral circuit region (right hand side of fig. 2F), recess amount of

element isolating portion equal zero, or relatively small.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9 and 21 are rejected under 35 U.S.C 103 as being unpatentable over Huang as applied to claims 1-8, 10-11, 20 above, and further in view of Nishioka 2002/0008019.

The difference between the references applied above and the instant claim(s) is: Huang teaches an embedding oxide film but does not specify the oxide is a HDP oxide. However, teaches at para. 6, an embedding oxide film is a HDP oxide. And, the selection of oxide density and coating thickness as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with HDP oxide as taught by Nishioka because higher density of oxide increases the insulation value.

Claims 23-27 are rejected under 35 U.S.C 103 as being unpatentable over Pividori as applied to claim 22 above, and further in view of Su 2002/0137282.

The difference between the references applied above and the instant claim(s) is: Su teaches a memory device includes memory area and peripheral area having an recessed embedding oxide film in the trench but does not specify memory structure. However, Su teaches at para. 2, and figs. 1-6, the memory structure is a flush memory having floating and control gate and arrange in parallel and orthogonal to each other for source/drain and word lines. And, the specific dimension of the recess, the width of isolation trench and coating thickness as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings of memory device in flush memory application as taught by Su because flush memory device is one of memory structure that can store information and the memory matrix is arranged in parallel and orthogonal direction so that bit and word can be accessed from x and Y direction, respectively.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is (703) 306-3329 and Fax number (703) 872-9306. Group receptionist telephone number 703-308-0956.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for this Group is (703) 872-9306.

hjt

3/18/04

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800